WHAT IS CLAIMED IS:

1. A method for providing a distributed high performance coherent memory with full error containment, comprising the steps of:

reading an error indication included in a packet, reflective of a current state of a unit;

determining if said current state of said unit is in error mode;

permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode;

driving an error indicator to a subject processor if said current state of unit is in error mode; and

ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode.

2. The method of claim 1 further including the step of:

ensuring that each member of a group of connected units, reads said error indication included in said packet, if said current state of a unit is in error mode.

3. The method of claim 1 further including the step of:

ensuring that each member of said group of connected units having at least one connected unit passes said error indication included in said packet if said current state of a unit is in error mode to a next member of said group of connected units.

4. The method of claim 1 wherein said error indication in said packet is in the form of an error bit.

5. The method of claim 1 wherein said error indication in said packet contained within a header of said packet.

6. The method of claim 1 further comprising the step of:
implementing a recovery routine by said subject processor.

7. The method of claim 1 wherein said reading step includes reading said error indication from an error bit.

8. The method of claim 1 further comprising the step of:
implementing a software recovery routine to clear said error mode.

9. The method of claim 1, further comprising the step of:
setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area.

10. The method of claim 9, wherein said error bit is provided as a fatal error bit.

11. The method of claim 9, wherein said error bit is provided as a shared memory bit, and wherein said unit comprises a shared memory area.

12 A distributed high performance coherent memory module with full error containment, comprising:

a reading module for reading an error indication included in a packet reflective of a current state of a unit;

a determination module for determining if said state of a unit is in error mode;

a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode;

a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode;

a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode; and

a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode.

13. The module of claim 12 further comprising:

a passing module for ensuring that each member of a group of connected units passes said error indication included in said packet, if said current state of a unit is in error mode, to a next unit member of group of connected units having at least one connected unit.

14. The module of claim 12 further comprising an error indication module for providing an error indication to be included in said packet reflective of the current state of a unit.

15 The module of claim 12 further comprising:

a processor recovery module for implementing a recovery routine by said subject processor.

16. The module of claim 12 further comprising:

a unit recovery module for implementing a software recovery routine to clear said error mode from said unit.

17. The module of claim 12 further comprising:

a shared memory error module for setting a shared memory error bit to be included in said packet for representing the presence of an error in a shared memory area.

18. The error indication module of claim 12 further comprising:

a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit; and

means for moving said error indication coextensive only with errors in particular data.

19. A system for error containment, said system comprising:

means for transporting error indications together with data which is in error; and

means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data.

20. A system for error containment as set forth in claim 19 further including:

means for propagating said error indications to next ones of said devices to which said error data must be delivered, said propagating occurring concurrently with error data delivery.